choice by swapping

devices with no other circuit redesign

- Tight I [2] parameter tolerance reduces system cost
  - Maximizes MOSFET and magnetics power delivery

hold-up time to reduce input bulk capacitance

- Self-biased: no bias winding or bias components

Enhanced Safety and Reliability Features

automatic recovery eliminates need for manual reset

- Improved auto-restart delivers <3% of maximum power
  in short circuit and open loop fault conditions
- Output overvoltage shutdown with optional Zener

optional resistor

- Very low component count enhances reliability and
  enables single-sided printed circuit board layout
- High bandwidth provides fast turn on with no overshoot
  and excellent transient load response
- Extended creepage between DRAIN and all other pins
  improves field reliability

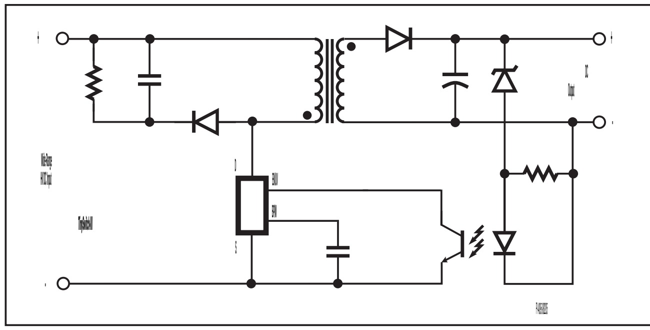
EcoSmart® – Extremely Energy Efficient

- Easily meets all global energy efficiency regulations

very light loads – ideal for mandatory CEC regulations

Applications

cameras, MP3/portable audio, shavers, etc.



OUTPUT POWER TABLE				
PRODUCT [3]	230 VAC ±15%		85-265 VAC	
	Adapter [1]	Peak or Open Frame [2]	Adapter [1]	Peak or Open Frame [2]
TNY274 P or G	6 W	11 W	5 W	8.5 W
TNY275 P or G	8.5 W	15 W	6 W	11.5 W
TNY276 P or G	10 W	19 W	7 W	15 W
TNY277 P or G	13 W	23.5 W	8 W	18 W
TNY278 P or G	16 W	28 W	10 W	21.5 W
TNY279 P or G	18 W	32 W	12 W	25 W
TNY280 P or G	20 W	36.5 W	14 W	28.5 W

Table 1. Notes: Minimum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient. Use of an external heatsink will increase power capability. Minimum peak power capability in any design or minimum continuous power in an open frame design (see Key Application Considerations). Packages: P: DIP-8C, G: SMD-8C. See Part Ordering Information.

- PC Standby and other auxiliary supplies
- DVD/PVR and other low power set top decoders
- Supplies for appliances, industrial systems, metering, etc.

Description

TinySwitch-III incorporates a 700 V power MOSFET, oscillator, high voltage switched current source, current limit (user selectable) and thermal shutdown circuitry. The IC family uses an ON/OFF control scheme and offers a design flexible solution with a low system cost and extended power capability.

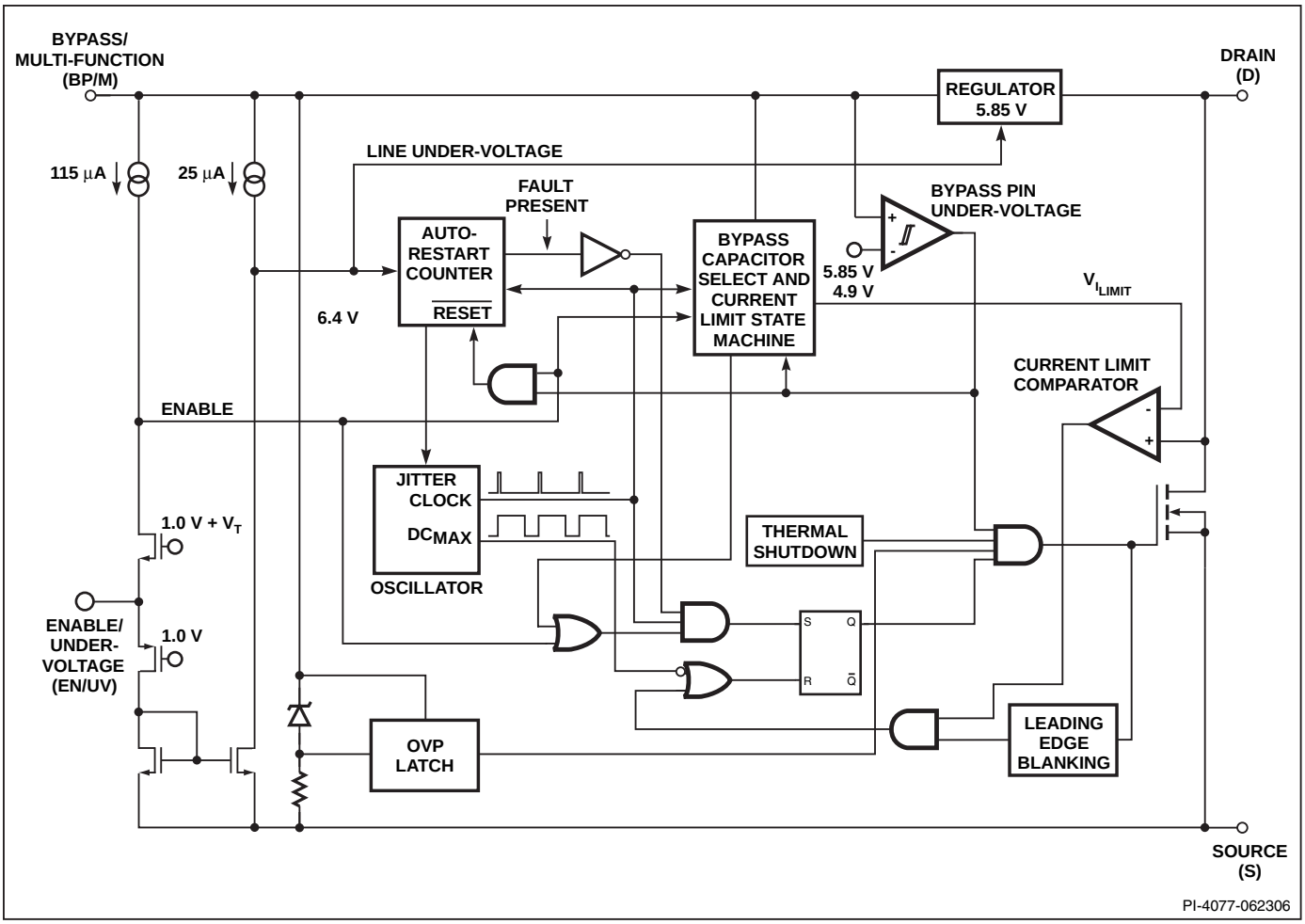


Figure 2. Functional Block Diagram.

Pin Functional Description

This pin is the power MOSFET drain connection. It provides internal operating current for both startup and steady-state operation.

This pin has multiple functions:

1. It is the connection point for an external bypass capacitor for the internally generated 5.85 V supply.
2. It is a mode selector for the current limit value, depending on the value of the capacitance added. Use of a 0.1 µF capacitor results in the standard current limit value. Use of a 1 µF capacitor results in the current limit being reduced to that of the next smaller device size. Use of a 10 µF capacitor results in the current limit being increased to that of the next larger device size for TNY275-280.
3. It provides a shutdown function. When the current into the bypass pin exceeds I_{SD}, the device latches off until the BP/M voltage drops below 4.9 V, during a power down. This can be used to provide an output overvoltage function with a Zener connected from the BP/M pin to a bias winding supply.

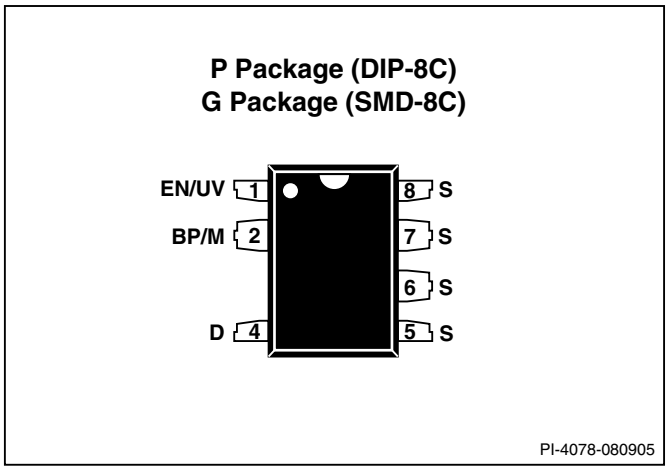


Figure 3. Pin Configuration.

This pin has dual functions: enable input and line undervoltage sense. During normal operation, switching of the power

MOSFET is controlled by this pin. MOSFET switching is terminated when a current greater than a threshold current is drawn from this pin. Switching resumes when the current being pulled from the pin drops to less than a threshold current. A modulation of the threshold current reduces group pulsing. The threshold current is between 75 µA and 115 µA.

The EN/UV pin also senses line undervoltage conditions through an external resistor connected to the DC line voltage. If there is no external resistor connected to this pin, *TinySwitch-III* detects its absence and disables the line undervoltage function.

This pin is internally connected to the output MOSFET source for high voltage power return and control circuit common.

TinySwitch-III Functional Description

TinySwitch-III combines a high voltage power MOSFET switch with a power supply controller in one device. Unlike conventional PWM (pulse width modulator) controllers, it uses a simple ON/OFF control to regulate the output voltage.

The controller consists of an oscillator, enable circuit (sense and logic), current limit state machine, 5.85 V regulator, BYPASS/MULTI-FUNCTION pin undervoltage, overvoltage circuit, and current limit selection circuitry, over- temperature protection, current limit circuit, leading edge blanking, and a 700 V power MOSFET. *TinySwitch-III* incorporates additional circuitry for line undervoltage sense, auto-restart, adaptive switching cycle on-time extension, and frequency jitter. Figure 2 shows the functional block diagram with the most important features.

The typical oscillator frequency is internally set to an average of 132 kHz. Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of each cycle.

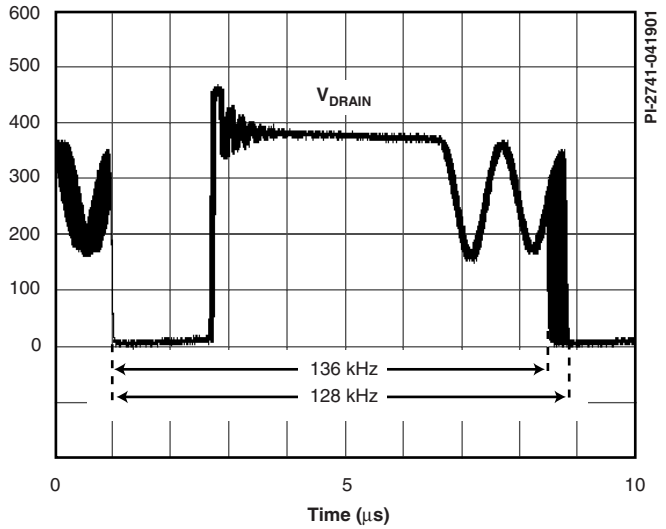


Figure 4. Frequency Jitter.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 8 kHz peak-to-peak, to minimize EMI emission. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter should be measured with the oscilloscope triggered at the falling edge of the DRAIN waveform. The waveform in Figure 4 illustrates the frequency jitter.

The enable input circuit at the EN/UV pin consists of a low impedance source follower output set at 1.2 V. The current through the source follower is limited to 115 µA. When the current out of this pin exceeds the threshold current, a low logic level (disable) is generated at the output of the enable circuit, until the current out of this pin is reduced to less than the threshold current. This enable circuit output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled). If low, the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the EN/UV pin voltage or current during the remainder of the cycle are ignored.

The current limit state machine reduces the current limit by discrete amounts at light loads when *TinySwitch-III* is likely to switch in the audible frequency range. The lower current limit raises the effective switching frequency above the audio range and reduces the transformer flux density, including the associated audible noise. The state machine monitors the sequence of enable events to determine the load condition and adjusts the current limit level accordingly in discrete amounts.

Under most operating conditions (except when close to no-load), the low impedance of the source follower keeps the voltage on the EN/UV pin from going much below 1.2 V in the disabled state. This improves the response time of the optocoupler that is usually connected to this pin.

The 5.85 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.85 V by drawing a current from the voltage on the DRAIN pin whenever the MOSFET is off. The BYPASS/MULTI-FUNCTION pin is the internal supply voltage node. When the MOSFET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows *TinySwitch-III* to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.4 V shunt regulator clamping the BYPASS/MULTI-FUNCTION pin at 6.4 V when current is provided to the BYPASS/MULTI-FUNCTION pin through an external resistor. This facilitates powering of *TinySwitch-III* externally through a bias winding to decrease the no-load consumption to well below 50 mW.

The BYPASS/MULTI-FUNCTION pin undervoltage circuitry disables the power MOSFET when the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady state operation. Once the BYPASS/MULTI-FUNCTION pin voltage drops below 4.9 V in steady state operation, it must rise back to 5.85 V to enable (turn-on) the power MOSFET.

The thermal shutdown circuitry senses the die temperature. The threshold is typically set at 142 °C with 75 °C hysteresis. When the die temperature rises above this threshold the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point it is re-enabled. A large hysteresis of 75 °C (typical) is provided to prevent overheating of the PC board due to a continuous fault condition.

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The current limit state machine reduces the current limit threshold by discrete amounts under medium and light loads.

The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and secondary-side rectifier reverse recovery time will not cause premature termination of the switching pulse.

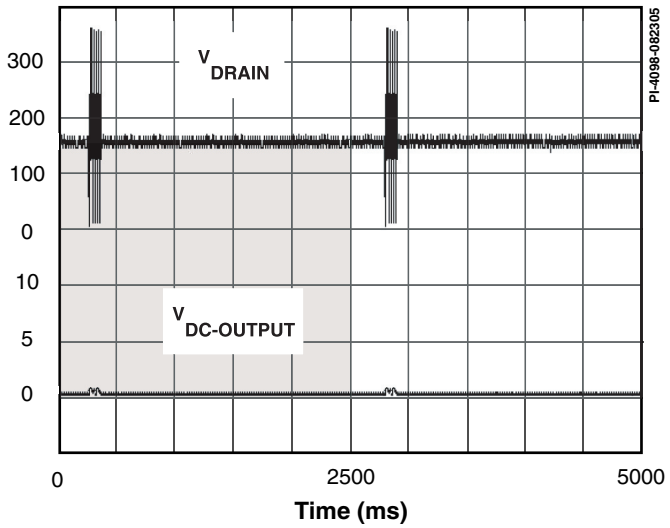


Figure 5. Auto-Restart Operation.

In the event of a fault condition such as output overload, output short circuit, or an open loop condition, *TinySwitch-III* enters into auto-restart operation. An internal counter clocked by the oscillator is reset every time the EN/UV pin is pulled low. If the EN/UV pin is not pulled low for 64 ms, the power MOSFET switching is normally disabled for 2.5 seconds (except in the case of line undervoltage condition, in which case it is disabled until the condition is removed). The auto-restart alternately enables and disables the switching of the power MOSFET until the fault condition is removed. Figure 5 illustrates auto-restart circuit operation in the presence of an output short circuit.

In the event of a line undervoltage condition, the switching of the power MOSFET is disabled beyond its normal 2.5 seconds until the line undervoltage condition ends.

Adaptive switching cycle on-time extension keeps the cycle on until current limit is reached, instead of prematurely terminating after the DC_{MAX} signal goes low. This feature reduces the minimum input voltage required to maintain regulation, extending hold-up time and minimizing the size of bulk capacitor required. The on-time extension is disabled during the startup of the power supply, until the power supply output reaches regulation.

The DC line voltage can be monitored by connecting an external resistor from the DC line to the EN/UV pin. During power up or when the switching of the power MOSFET is disabled in auto-restart, the current into the EN/UV pin must exceed 25 µA to initiate switching of the power MOSFET. During power up, this is accomplished by holding the BYPASS/MULTI-FUNCTION pin to 4.9 V while the line undervoltage condition exists. The BYPASS/MULTI-FUNCTION pin then rises from 4.9 V to 5.85 V when the line undervoltage condition goes away. When the switching of the power MOSFET is disabled in auto-restart mode and a line undervoltage condition exists, the auto-restart counter is stopped. This stretches the disable time beyond its normal 2.5 seconds until the line undervoltage condition ends.

The line undervoltage circuit also detects when there is no external resistor connected to the EN/UV pin (less than ~2 µA into the pin). In this case the line undervoltage function is disabled.

TinySwitch-III Operation

TinySwitch-III devices operate in the current limit mode. When enabled, the oscillator turns the power MOSFET on at the beginning of each cycle. The MOSFET is turned off when the current ramps up to the current limit or when the DC_{MAX} limit is reached. Since the highest current limit level and frequency of a *TinySwitch-III* design are constant, the power delivered to the

load is proportional to the primary inductance of the transformer and peak primary current squared. Hence, designing the supply involves calculating the primary inductance of the transformer for the maximum output power required. If the *TinySwitch-III* is appropriately chosen for the power level, the current in the calculated inductance will ramp up to current limit before the DC_{MAX} limit is reached.

TinySwitch-III senses the EN/UV pin to determine whether or not to proceed with the next switching cycle. The sequence of cycles is used to determine the current limit. Once a cycle is started, it always completes the cycle (even when the EN/UV pin changes state half way through the cycle). This operation results in a power supply in which the output voltage ripple is determined by the output capacitor, amount of energy per switch cycle and the delay of the feedback.

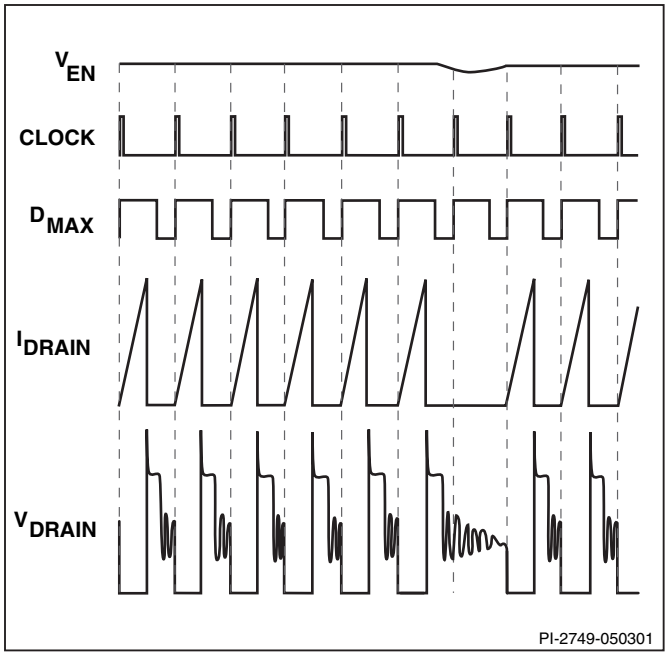


Figure 6. Operation at Near Maximum Loading.

The EN/UV pin signal is generated on the secondary by comparing the power supply output voltage with a reference voltage. The EN/UV pin signal is high when the power supply output voltage is less than the reference voltage.

In a typical implementation, the EN/UV pin is driven by an optocoupler. The collector of the optocoupler transistor is connected to the EN/UV pin and the emitter is connected to the SOURCE pin. The optocoupler LED is connected in series with a Zener diode across the DC output voltage to be regulated. When the output voltage exceeds the target regulation voltage level (optocoupler LED voltage drop plus Zener voltage), the optocoupler LED will start to conduct, pulling the EN/UV pin low. The Zener diode can be replaced by a TL431 reference circuit for improved accuracy.

The internal clock of the *TinySwitch-III* runs all the time. At the beginning of each clock cycle, it samples the EN/UV pin to decide whether or not to implement a switch cycle, and based on the sequence of samples over multiple cycles, it determines the appropriate current limit. At high loads, the state machine sets the current limit to its highest value. At lighter loads, the state machine sets the current limit to reduced values.

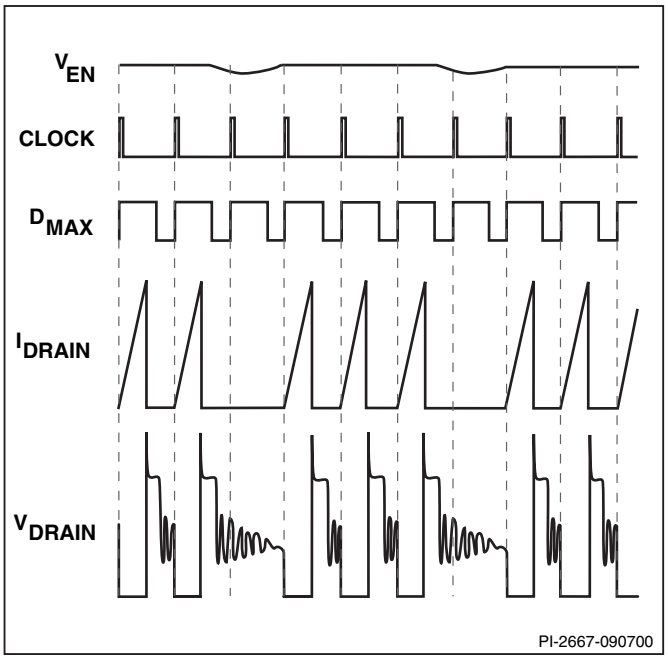


Figure 7. Operation at Moderately Heavy Loading.

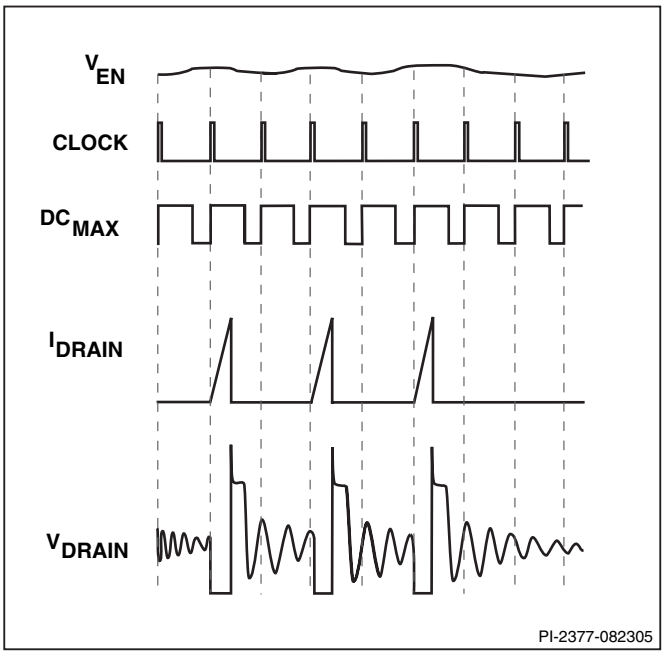


Figure 8. Operation at Medium Loading.

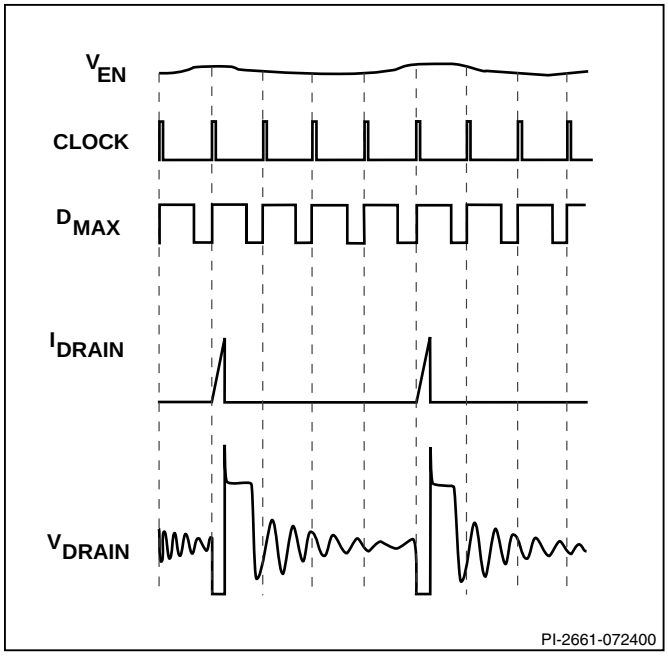


Figure 9. Operation at Very Light Load.

At near maximum load, *TinySwitch-III* will conduct during nearly all of its clock cycles (Figure 6). At slightly lower load, it will "skip" additional cycles in order to maintain voltage regulation at the power supply output (Figure 7). At medium loads, cycles will be skipped and the current limit will be reduced (Figure 8). At very light loads, the current limit will be reduced even further (Figure 9). Only a small percentage of cycles will occur to satisfy the power consumption of the power supply.

The response time of the ON/OFF control scheme is very fast compared to PWM control. This provides tight regulation and excellent transient response.

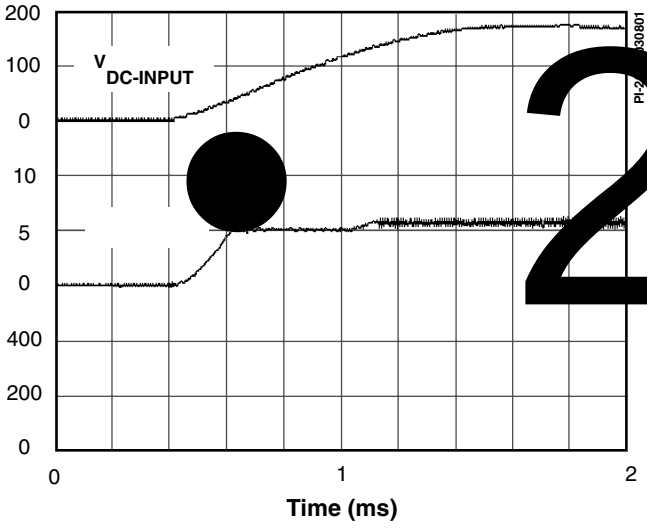


Figure 10. Power Up with Optional External UV Resistor (4 MΩ) Connected to EN/UV Pin.

Figure 11. Power Up Without Optional External UV Resistor Connected to EN/UV Pin.

Figure 12. Normal Power Down Timing (without UV).

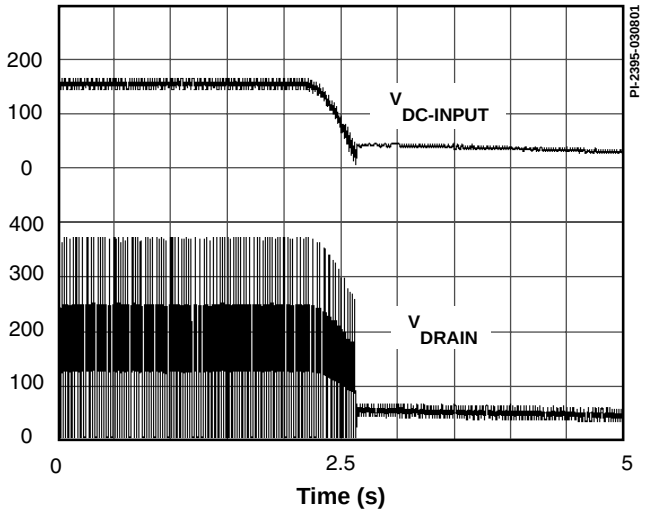


Figure 13. Slow Power Down Timing with Optional External (4 MΩ) UV Resistor Connected to EN/UV Pin.

The *TinySwitch-III* requires only a 0.1 µF capacitor on the BYPASS/MULTI-FUNCTION pin to operate with standard current limit. Because of its small size, the time to charge this capacitor is kept to an absolute minimum, typically 0.6 ms. The time to charge will vary in proportion to the BYPASS/MULTI-FUNCTION pin capacitor value when selecting different current limits. Due to the high bandwidth of the ON/OFF feedback, there is no overshoot at the power supply output. When an external resistor (4 MΩ) is connected from the positive DC input to the EN/UV pin, the power MOSFET switching will be delayed during power up until the DC line voltage exceeds the threshold (100 V). Figures 10 and 11 show the power up timing waveform in applications with and without an external resistor (4 MΩ) connected to the EN/UV pin.

Under startup and overload conditions, when the conduction time is less than 400 ns, the device reduces the switching frequency to maintain control of the peak drain current.

During power down, when an external resistor is used, the power MOSFET will switch for 64 ms after the output loses regulation. The power MOSFET will then remain off without any glitches since the undervoltage function prohibits restart when the line voltage is low.

Figure 12 illustrates a typical power down timing waveform. Figure 13 illustrates a very slow power down timing waveform as in standby applications. The external resistor (4 MΩ) is connected to the EN/UV pin in this case to prevent unwanted restarts.

No bias winding is needed to provide power to the chip because it draws the power directly from the DRAIN pin (see Functional Description above). This has two main benefits. First, for a nominal application, this eliminates the cost of a bias winding and associated components. Secondly, for battery charger applications, the current-voltage characteristic often allows the output voltage to fall close to zero volts while still delivering power. *TinySwitch-III* accomplishes this without a forward bias winding and its many associated components. For applications that require very low no-load power consumption (50 mW), a resistor from a bias winding to the BYPASS/MULTI-FUNCTION pin can provide the power to the chip. The minimum recommended current supplied is 1 mA. The BYPASS/MULTI-FUNCTION pin in this case will be clamped at 6.4 V. This method will eliminate the power draw from the DRAIN pin, thereby reducing the no-load power consumption and improving full-load efficiency.

Each switching cycle is terminated when the DRAIN current reaches the current limit of the device. Current limit operation provides good line ripple rejection and relatively constant power delivery independent of input voltage.

The BYPASS/MULTI-FUNCTION pin can use a ceramic capacitor as small as 0.1 µF for decoupling the internal power supply of the device. A larger capacitor size can be used to adjust the current limit. For TNY275-280, a 1 µF BP/M pin capacitor will select a lower current limit equal to the standard current limit of the next smaller device and a 10 µF BP/M pin capacitor will select a higher current limit equal to the standard current limit of the next larger device. The higher current limit level of the TNY280 is set to 850 mA typical. The TNY274 MOSFET does not have the capability for increased current limit so this feature is not available in this device.

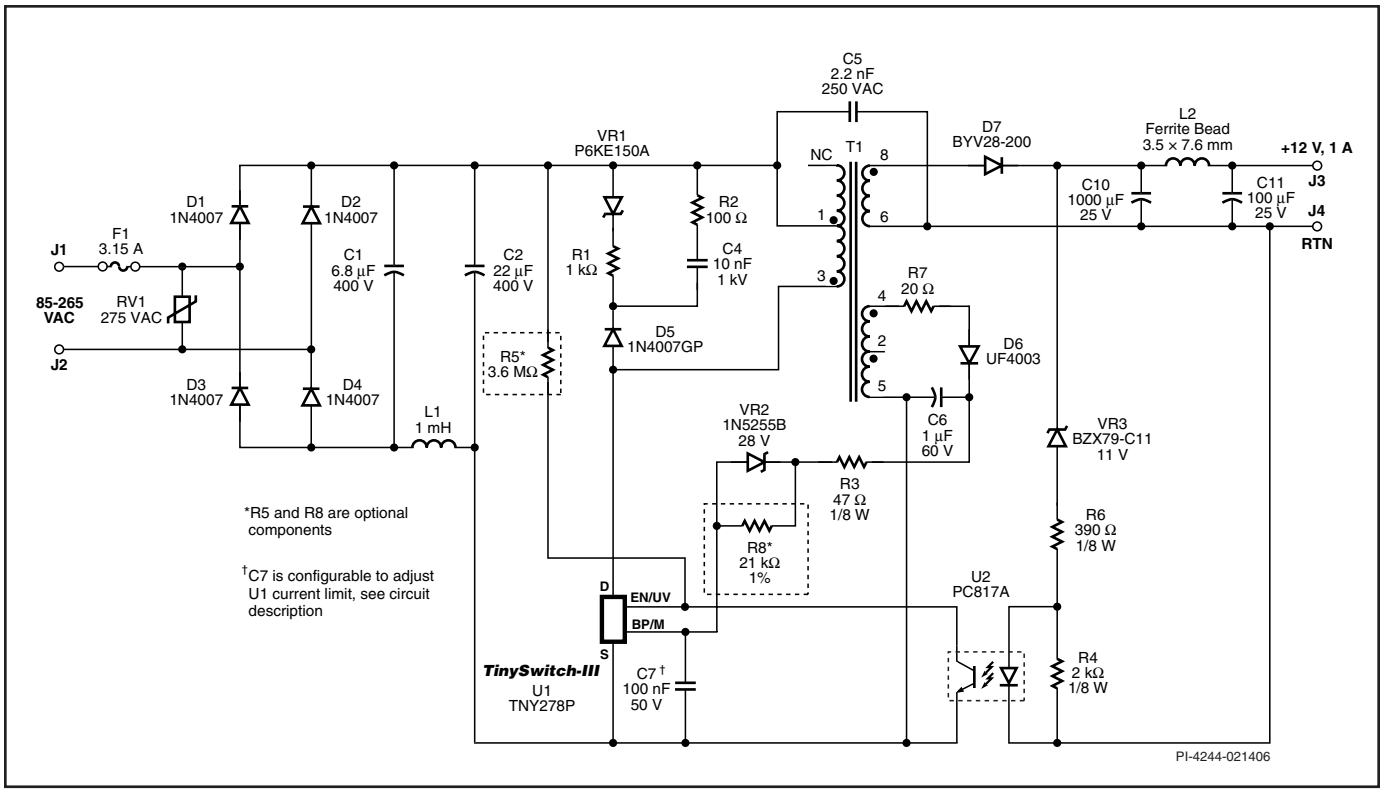


Figure 14. TNY278P, 12 V, 1 A Universal Input Power Supply.

Applications Example

The circuit shown in Figure 14 is a low cost, high efficiency, flyback power supply designed for 12 V, 1 A output from universal input using the TNY278.

The supply features undervoltage lockout, primary sensed output overvoltage latching shutdown protection, high efficiency (>80%), and very low no-load consumption (<50 mW at 265 VAC). Output regulation is accomplished using a simple zener reference and optocoupler feedback.

The rectified and filtered input voltage is applied to the primary winding of T1. The other side of the transformer primary is driven by the integrated MOSFET in U1. Diode D5, C2, R1, R2, and VR1 comprise the clamp circuit, limiting the leakage inductance turn-off voltage spike on the DRAIN pin to a safe value. The use of a combination a Zener clamp and parallel RC optimizes both EMI and energy efficiency. Resistor R2 allows the use of a slow recovery, low cost, rectifier diode by limiting the reverse current through D5. The selection of a slow diode also improves efficiency and conducted EMI but should be a glass passivated type, with a specified recovery time of ≤2 µs.

The output voltage is regulated by the Zener diode VR3. When the output voltage exceeds the sum of the Zener and optocoupler LED forward drop, current will flow in the optocoupler LED. This will cause the transistor of the optocoupler to sink current. When this current exceeds the ENABLE pin threshold current the next switching cycle is inhibited. When the output voltage falls below the feedback threshold, a conduction cycle is allowed to occur and, by adjusting the number of enabled cycles, output regulation is maintained. As the load reduces, the number of enabled cycles decreases, lowering the effective switching frequency and scaling switching losses with load. This provides almost constant efficiency down to very light loads, ideal for meeting energy efficiency requirements.

As the *TinySwitch-III* devices are completely self-powered, there is no requirement for an auxiliary or bias winding on the transformer. However by adding a bias winding, the output overvoltage protection feature can be configured, protecting the load against open feedback loop faults.

When an overvoltage condition occurs, such that bias voltage exceeds the sum of VR2 and the BYPASS/MULTIFUNCTION (BP/M) pin voltage (28 V+5.85 V), current begins to flow into the BP/M pin. When this current exceeds I_{SD} the internal latching shutdown circuit in *TinySwitch-III* is activated. This condition is reset when the BP/M pin voltage drops below 2.6 V after removal of the AC input. In the example shown, on opening the loop, the OVP trips at an output of 17 V.

For lower no-load input power consumption, the bias winding may also be used to supply the *TinySwitch-III* device. Resistor R8 feeds current into the BP/M pin, inhibiting the internal high voltage current source that normally maintains the BP/M pin capacitor voltage (C7) during the internal MOSFET off time. This reduces the no-load consumption of this design from 140 mW to 40 mW at 265 VAC.

Undervoltage lockout is configured by R5 connected between the DC bus and EN/UV pin of U1. When present, switching is inhibited until the current in the EN/UV pin exceeds 25 µA. This allows the startup voltage to be programmed within the normal operating input voltage range, preventing glitching of the output under abnormal low voltage conditions and also on removal of the AC input.

In addition to the simple input pi filter (C1, L1, C2) for differential mode EMI, this design makes use of *E-Shield*™ shielding techniques in the transformer to reduce common mode EMI displacement currents, and R2 and C4 as a damping network to reduce high frequency transformer ringing. These techniques, combined with the frequency jitter of TNY278, give excellent conducted and radiated EMI performance with this design achieving >12 dBµV of margin to EN55022 Class B conducted EMI limits.

For design flexibility the value of C7 can be selected to pick one of the 3 current limits options in U1. This allows the designer to select the current limit appropriate for the application.

- Standard current limit (I_{LIMIT}) is selected with a 0.1 µF BP/M pin capacitor and is the normal choice for typical enclosed adapter applications.
- When a 1 µF BP/M pin capacitor is used, the current limit is reduced ($I_{LIMITred}$ or I_{LIMIT}-1) offering reduced RMS device currents and therefore improved efficiency, but at the expense of maximum power capability. This is ideal for thermally challenging designs where dissipation must be minimized.
- When a 10 µF BP/M pin capacitor is used, the current limit is increased ($I_{LIMITinc}$ or I_{LIMIT}+1), extending the power capability for applications requiring higher peak power or continuous power where the thermal conditions allow.

Further flexibility comes from the current limits between adjacent *TinySwitch-III* family members being compatible. The reduced current limit of a given device is equal to the standard current limit of the next smaller device and the increased current limit is equal to the standard current limit of the next larger device.

Key Application Considerations

TinySwitch-III Design Considerations

The data sheet output power table (Table 1) represents the minimum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 100 V or higher for 85 VAC input, or 220 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be sized to meet these criteria for AC input designs.
2. Efficiency of 75%.
3. Minimum data sheet value of I^2f.
4. Transformer primary inductance tolerance of ±10%.
5. Reflected output voltage (V_{OR}) of 135 V.
6. Voltage only output of 12 V with a fast PN rectifier diode.
7. Continuous conduction mode operation with transient K_P* value of 0.25.
8. Increased current limit is selected for peak and open frame power columns and standard current limit for adapter columns.
9. The part is board mounted with SOURCE pins soldered to a sufficient area of copper and/or a heatsink is used to keep the SOURCE pin temperature at or below 110 °C.
10. Ambient temperature of 50 °C for open frame designs and 40 °C for sealed adapters.

*Below a value of 1, K_p is the ratio of ripple to peak primary current. To prevent reduced power capability due to premature termination of switching cycles a transient K_p limit of ≥0.25 is recommended. This prevents the initial current limit (I_{INIT}) from being exceeded at MOSFET turn on.

For reference, Table 2 provides the minimum practical power delivered from each family member at the three selectable current limit values. This assumes open frame operation (not thermally limited) and otherwise the same conditions as listed above. These numbers are useful to identify the correct current limit to select for a given device and output power requirement.

The output overvoltage protection provided by *TinySwitch-III* uses an internal latch that is triggered by a threshold current of approximately 5.5 mA into the BP/M pin. In addition to an internal filter, the BP/M pin capacitor forms an external filter providing noise immunity from inadvertent triggering. For the bypass capacitor to be effective as a high frequency filter, the capacitor should be located as close as possible to the SOURCE and BP/M pins of the device.

OUTPUT POWER TABLE						
PRODUCT	230 VAC ±15%			85-265 VAC		
	I_{LIMIT}-1	I_{LIMIT}	I_{LIMIT}+1	I_{LIMIT}-1	I_{LIMIT}	I_{LIMIT}+1
TNY274 P or G	9	10.9	9.1	7.1	8.5	7.1
TNY275 P or G	10.8	12	15.1	8.4	9.3	11.8
TNY276 P or G	11.8	15.3	19.4	9.2	11.9	15.1
TNY277 P or G	15.1	19.6	23.7	11.8	15.3	18.5
TNY278 P or G	19.4	24	28	15.1	18.6	21.8
TNY279 P or G	23.7	28.4	32.2	18.5	22	25.2
TNY280 P or G	28	32.7	36.6	21.8	25.4	28.5

Table 2. Minimum Practical Power at Three Selectable Current Limit Levels.

For best performance of the OVP function, it is recommended that a relatively high bias winding voltage is used, in the range of 15 V-30 V. This minimizes the error voltage on the bias winding due to leakage inductance and also ensures adequate voltage during no-load operation from which to supply the BP/M pin for reduced no-load consumption.

Selecting the Zener diode voltage to be approximately 6 V above the bias winding voltage (28 V for 22 V bias winding) gives good OVP performance for most designs, but can be adjusted to compensate for variations in leakage inductance. Adding additional filtering can be achieved by inserting a low value (10 Ω to 47 Ω) resistor in series with the bias winding diode and/or the OVP Zener as shown by R7 and R3 in Figure 14. The resistor in series with the OVP Zener also limits the maximum current into the BP/M pin.

As *TinySwitch-III* is self-powered from the BP/M pin capacitor, there is no need for an auxillary or bias winding to be provided on the transformer for this purpose. Typical no-load consumption when self-powered is <150 mW at 265 VAC input. The addition of a bias winding can reduce this down to <50 mW by supplying the *TinySwitch-III* from the lower bias voltage and inhibiting the internal high voltage current source. To achieve this, select the value of the resistor (R8 in Figure 14) to provide the data sheet DRAIN supply current. In practice, due to the reduction of the bias voltage at low load, start with a value equal to 40% greater than the data sheet maximum current, and then increase the value of the resistor to give the lowest no-load consumption.

The cycle skipping mode of operation used in *TinySwitch-III* can generate audio frequency components in the transformer. To limit this audible noise generation the transformer should be designed such that the peak core flux density is below 3000 Gauss (300 mT). Following this guideline and using the standard transformer production technique of dip varnishing practically eliminates audible noise. Vacuum impregnation of the transformer should not be used due to the high primary capacitance and increased losses that result. Higher flux densities are possible, however careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

TinySwitch-III Layout Considerations

See Figure 15 for a recommended circuit board layout for *TinySwitch-III*.

Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

The BP/M pin capacitor should be located as near as possible to the BP/M and SOURCE pins.

Keep traces connected to the EN/UV pin short and, as far as is practical, away from all other traces and nodes above source potential including, but not limited to, the BYPASS and DRAIN pins.

The area of the primary loop that connects the input filter capacitor, transformer primary and *TinySwitch-III* together should be kept as small as possible.

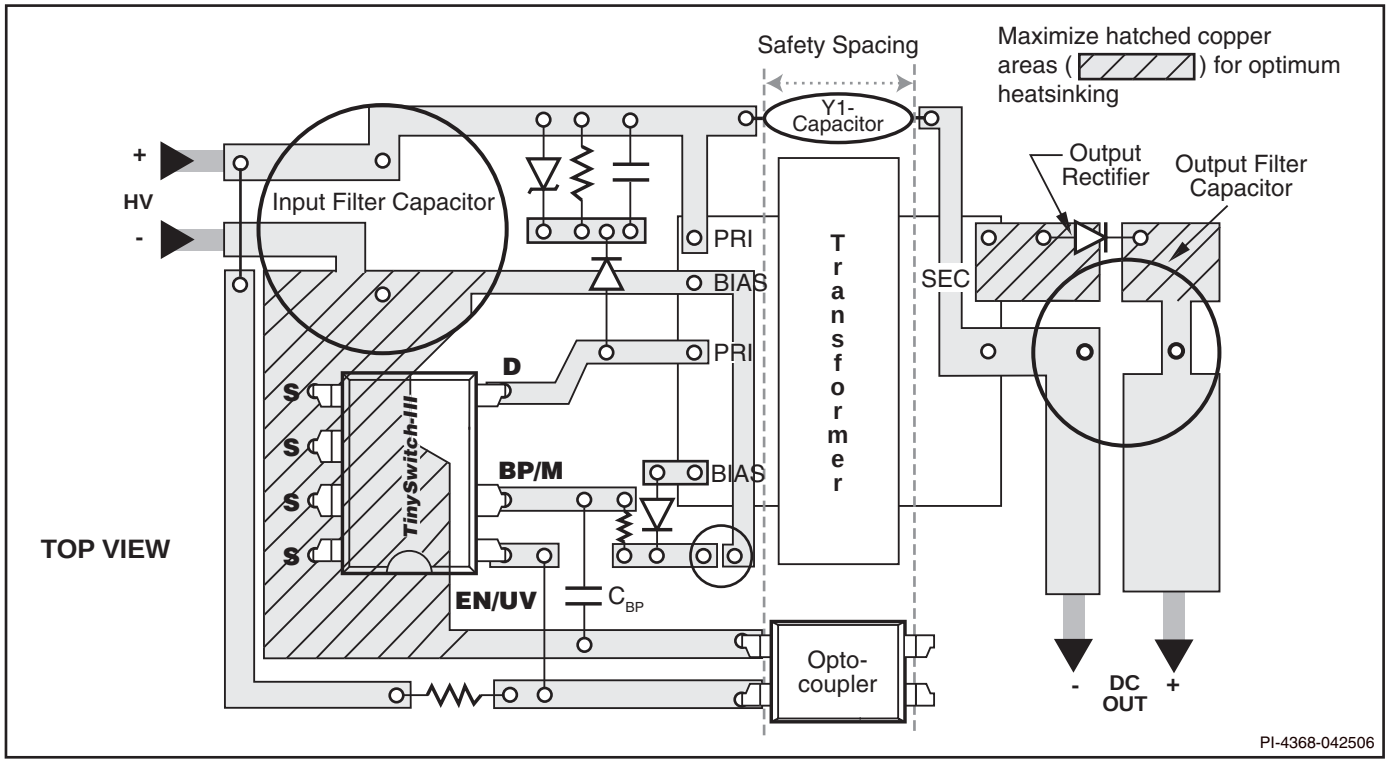


Figure 15. Recommended Circuit Board Layout for TinySwitch-III with Undervoltage Lock Out Resistor.

A clamp is used to limit peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and *TinySwitch-III.*

The four SOURCE pins are internally connected to the IC lead frame and provide the main path to remove heat from the device. Therefore all the SOURCE pins should be connected to a copper area underneath the *TinySwitch-III* to act not only as a single point ground, but also as a heatsink. As this area is connected to the quiet source node, this area should be maximized for good heatsinking. Similarly for axial output diodes, maximize the PCB area connected to the cathode.

The placement of the Y-capacitor should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common mode surge currents away from the *TinySwitch-III* device. Note – if an input π (C, L, C) EMI filter is used then the inductor in the filter should be placed between the negative terminals of the input filter capacitors.

Place the optocoupler physically close to the *TinySwitch-III* to minimizing the primary-side trace lengths. Keep the high current, high voltage drain and clamp traces away from the optocoupler to prevent noise pick up.

For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor, should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heatsinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high frequency radiated EMI.

TinySwitch-III is designed to optimize energy efficiency across the power range and particularly in standby/no-load conditions. Current consumption has therefore been minimized to achieve this performance. The EN/UV pin undervoltage feature for example has a low threshold (~1 µA) to detect whether an undervoltage resistor is present.

Parasitic leakage currents into the EN/UV pin are normally well below this 1 µA threshold when PC board assembly is in a well controlled production facility. However, high humidity conditions together with board and/or package contamination,

either from no-clean flux or other contaminants, can reduce the surface resistivity enough to allow parasitic currents >1 µA to flow into the EN/UV pin. These currents can flow from higher voltage exposed solder pads close to the EN/UV pin such as the BP/M pin solder pad preventing the design from starting up. Designs that make use of the undervoltage lockout feature by connecting a resistor from the high voltage rail to the EN/UV pin are not affected.

If the contamination levels in the PC board assembly facility are unknown, the application is open frame or operates in a high pollution degree environment and the design does not make use of the undervoltage lockout feature, then an optional 390 kΩ resistor should be added from EN/UV pin to SOURCE pin to ensure that the parasitic leakage current into the EN/UV pin is well below 1 µA.

Note that typical values for surface insulation resistance (SIR) where no-clean flux has been applied according to the suppliers' guidelines are >>10 MΩ and do not cause this issue.

Quick Design Checklist

As with any power supply design, all *TinySwitch-III* designs should be verified on the bench to make sure that component specifications are not exceeded under worst case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 650 V at highest input voltage and peak (overload) output power. The 50 V margin to the 700 V BV_{DSS} specification gives margin for design variation.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading edge current spikes at startup. Repeat under steady state conditions and verify that the leading edge current spike event is below $I_{LIMIT(Min)}$ at the end of the $t_{LEB(Min)}$. Under all conditions, the maximum drain current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for *TinySwitch-III*, transformer, output diode, and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of *TinySwitch-III* as specified in the data sheet. Under low line, maximum power, a maximum *TinySwitch-III* SOURCE pin temperature of 110 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools is available at the Power Integrations website: *www.powerint.com.*

ABSOLUTE MAXIMUM RATINGS(1,5)

DRAIN Voltage .....-0.3 V to 700 V
DRAIN Peak Current: TNY274.....400 (750) mA(2)
TNY275.....560 (1050) mA(2)
TNY276.....720 (1350) mA(2)
TNY277.....880 (1650) mA(2)
TNY278.....1040 (1950) mA(2)
TNY279 ..... 1200 (2250) mA(2)
TNY280 ..... 1360 (2550) mA(2)
EN/UV Voltage ..... -0.3 V to 9 V
EN/UV Current ..... 100 mA
BP/M Voltage .....-0.3 V to 9 V
Storage Temperature .....-65 °C to 150 °C
Operating Junction Temperature(3) .....-40 °C to 150 °C
Lead Temperature(4) ..... 260 °C

1. All voltages referenced to SOURCE, T_A = 25 °C.
2. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
3. Normally limited by internal circuitry.
4. 1/16 in. from case for 5 seconds.
5. Maximum ratings specified may be applied one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE

Thermal Impedance: P or G Package:
(θ_{JA}) ..... 70 °C/W(2); 60 °C/W(3)
(θ_{JC})(1) ..... 11 °C/W

1. Measured on the SOURCE pin close to plastic interface.
2. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
3. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS							
Output Frequency in Standard Mode	f_{OSC}	T_J = 25 °C See Figure 4	Average	124	132	140	kHz
			Peak-to-peak Jitter		8		
Maximum Duty Cycle	DC_{MAX}	S1 Open		62	65		%
EN/UV Pin Upper Turnoff Threshold Current	I_{DIS}			-150	-115	-90	µA
EN/UV Pin Voltage	V_{EN}	$I_{EN/UV}$ = 25 µA		1.8	2.2	2.6	V
		$I_{EN/UV}$ = -25 µA		0.8	1.2	1.6	
DRAIN Supply Current	I_{S1}	EN/UV Current > I_{DIS} (MOSFET Not Switching) See Note A			290		µA
	I_{S2}	EN/UV Open (MOSFET Switching at f_{OSC}) See Note B	TNY274		275	360	µA
			TNY275		295	400	
			TNY276		310	430	
			TNY277		365	460	
			TNY278		445	540	
			TNY279		510	640	
			TNY280		630	760	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS (cont.)							
BP/M Pin Charge Current	I_{CH1}	$V_{BP/M}$ = 0 V, T_J = 25 °C See Note C, D	TNY274	-6	-3.8	-1.8	mA
			TNY275-279	-8.3	-5.4	-2.5	
			TNY280	-9.7	-6.8	-3.9	
	I_{CH2}	$V_{BP/M}$ = 4 V, T_J = 25 °C See Note C, D	TNY274	-4.1	-2.3	-1	
			TNY275-279	-5	-3.5	-1.5	
			TNY280	-6.6	-4.6	-2.1	
BP/M Pin Voltage	$V_{BP/M}$	See Note C		5.6	5.85	6.15	V
BP/M Pin Voltage Hysteresis	$V_{BP/MH}$			0.80	0.95	1.20	V
BP/M Pin Shunt Voltage	V_{SHUNT}	I_{BP} = 2 mA		6.0	6.4	6.7	V
EN/UV Pin Line Undervoltage Threshold	I_{LUV}	T_J = 25 °C		22.5	25	27.5	µA
CIRCUIT PROTECTION							
Standard Current Limit (BP/M Capacitor = 0.1 µF) See Note D	I_{LIMIT}	di/dt = 50 mA/µs T_J = 25 °C See Note E	TNY274P	233	250	267	mA
			TNY274G	233	250	273	
		di/dt = 55 mA/µs T_J = 25 °C See Note E	TNY275P	256	275	294	
			TNY275G	256	275	300	
		di/dt = 70 mA/µs T_J = 25 °C See Note E	TNY276P	326	350	374	
			TNY276G	326	350	382	
		di/dt = 90 mA/µs T_J = 25 °C See Note E	TNY277P	419	450	481	
			TNY277G	419	450	491	
		di/dt = 110 mA/µs T_J = 25 °C See Note E	TNY278P	512	550	588	
			TNY278G	512	550	600	
		di/dt = 130 mA/µs T_J = 25 °C See Note E	TNY279P	605	650	695	
			TNY279G	605	650	709	
		di/dt = 150 mA/µs T_J = 25 °C See Note E	TNY280P	698	750	802	
			TNY280G	698	750	818	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)		Min	Typ	Max	Units
CIRCUIT PROTECTION (cont.)							
Reduced Current Limit (BP/M Capacitor = 1 µF) See Note D	$I_{LIMITred}$	di/dt = 50 mA/µs T_J = 25 °C See Note E	TNY274P	196	210	233	mA
			TNY274G	196	210	237	
		di/dt = 55 mA/µs T_J = 25 °C See Note E	TNY275P	233	250	277	
			TNY275G	233	250	283	
		di/dt = 70 mA/µs T_J = 25 °C See Notes E	TNY276P	256	275	305	
			TNY276G	256	275	311	
		di/dt = 90 mA/µs T_J = 25 °C See Notes E	TNY277P	326	350	388	
			TNY277G	326	350	396	
		di/dt = 110 mA/µs T_J = 25 °C See Notes E	TNY278P	419	450	499	
			TNY278G	419	450	509	
		di/dt = 130 mA/µs T_J = 25 °C See Notes E	TNY279P	512	550	610	
			TNY279G	512	550	622	
		di/dt = 150 mA/µs T_J = 25 °C See Notes E	TNY280P	605	650	721	
			TNY280G	605	650	735	
Increased Current Limit (BP/M Capacitor = 10 µF) See Note D	$I_{LIMITinc}$	di/dt = 50 mA/µs T_J = 25 °C See Notes E, F	TNY274P	196	210	233	mA
			TNY274G	196	210	237	
		di/dt = 55 mA/µs T_J = 25 °C See Notes E	TNY275P	326	350	388	
			TNY275G	326	350	396	
		di/dt = 70 mA/µs T_J = 25 °C See Notes E	TNY276P	419	450	499	
			TNY276G	419	450	509	
		di/dt = 90 mA/µs T_J = 25 °C See Notes E	TNY277P	512	550	610	
			TNY277G	512	550	622	
		di/dt = 110 mA/µs T_J = 25 °C See Notes E	TNY278P	605	650	721	
			TNY278G	605	650	735	
		di/dt = 130 mA/µs T_J = 25 °C See Notes E	TNY279P	698	750	833	
			TNY279G	698	750	848	
		di/dt = 150 mA/µs T_J = 25 °C See Notes E	TNY280P	791	850	943	
			TNY280G	791	850	961	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)		Min	Typ	Max	Units
CIRCUIT PROTECTION (cont.)							
Power Coefficient	I^2f	Standard Current Limit, $I^2f = I_{LIMIT(TYP)}^2 \times f_{OSC(TYP)}$	TNY274-280P	0.9 × I^2f	I^2f	1.12 × I^2f	A^2Hz
			TNY274-280G	0.9 × I^2f	I^2f	1.16 × I^2f	
		Reduced Current Limit, $I^2f = I_{LIMITred(TYP)}^2 \times f_{OSC(TYP)}$	TNY274-280P	0.9 × I^2f	I^2f	1.16 × I^2f	
			TNY274-280G	0.9 × I^2f	I^2f	1.20 × I^2f	
		Increased Current Limit, $I^2f = I_{LIMITinc(TYP)}^2 \times f_{OSC(TYP)}$	TNY274-280P	0.9 × I^2f	I^2f	1.16 × I^2f	
			TNY274-280G	0.9 × I^2f	I^2f	1.20 × I^2f	
Initial Current Limit	I_{INIT}	See Figure 19 T_J = 25 °C, See Note G		0.75 × $I_{LIMIT(MIN)}$			mA
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note G		170	215		ns
Current Limit Delay	t_{ILD}	T_J = 25 °C See Note G, H			150		ns
Thermal Shut-down Temperature	T_{SD}			135	142	150	°C
Thermal Shut-down Hysteresis	T_{SDH}				75		°C
BP/M Pin Shut-down Threshold Current	I_{SD}			4	6.5	9	mA
BP/M Pin Power up Reset Thresh-old Voltage	$V_{BP/M(RESET)}$			1.6	2.6	3.6	V
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	TNY274 I_D = 25 mA	T_J = 25 °C		28	32	Ω
			T_J = 100 °C		42	48	
		TNY275 I_D = 28 mA	T_J = 25 °C		19	22	
			T_J = 100 °C		29	33	
		TNY276 I_D = 35 mA	T_J = 25 °C		14	16	
			T_J = 100 °C		21	24	

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 16 (Unless Otherwise Specified)		Min	Typ	Max	Units
OUTPUT (cont.)							
ON-State Resistance	$R_{DS(ON)}$	TNY277 I_D = 45 mA	T_J = 25 °C		7.8	9.0	Ω
			T_J = 100 °C		11.7	13.5	
		TNY278 I_D = 55 mA	T_J = 25 °C		5.2	6.0	
			T_J = 100 °C		7.8	9.0	
		TNY279 I_D = 65 mA	T_J = 25 °C		3.9	4.5	
			T_J = 100 °C		5.8	6.7	
		TNY280 I_D = 75 mA	T_J = 25 °C		2.6	3.0	
			T_J = 100 °C		3.9	4.5	
OFF-State Drain Leakage Current	I_{DSS1}	$V_{BP/M}$ = 6.2 V $V_{EN/UV}$ = 0 V V_{DS} = 560 V T_J = 125 °C See Note I	TNY274-276			50	µA
			TNY277-278			100	
			TNY279-280			200	
	I_{DSS2}	$V_{BP/M}$ = 6.2 V $V_{EN/UV}$ = 0 V	V_{DS} = 375 V, T_J = 50 °C See Note G, I		15		
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, $V_{EN/UV}$ = 0 V, See Note J, T_J = 25 °C		700			V
DRAIN Supply Voltage				50			V
Auto-Restart ON-Time at f_{OSC}	t_{AR}	T_J = 25 °C See Note K			64		ms
Auto-Restart Duty Cycle	DC_{AR}	T_J = 25 °C			3		%

NOTES:

A. I_{S1} is an accurate estimate of device controller current consumption at no-load, since operating frequency is so low under these conditions. Total device consumption at no-load is the sum of I_{S1} and I_{DSS2}.

B Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BP/M pin current at 6.1 V.

C. BP/M pin is not intended for sourcing supply current to external circuitry.

D. To ensure correct current limit it is recommended that nominal 0.1 µF / 1 µF / 10 µF capacitors are used. In addition, the BP/M capacitor value tolerance should be equal or better than indicated below across the ambient temperature range of the target application. The minimum and maximum capacitor values are guaranteed by characterization.

Nominal BP/M Pin Cap Value	Tolerance Relative to Nominal Capacitor Value	
	Min	MAX
0.1 µF	-60%	+100%
1 µF	-50%	+100%
10 µF	-50%	NA

E. For current limit at other di/dt values, refer to Figure 23.

F. TNY274 does not set an increased current limit value, but with a 10 µF BP/M pin capacitor the current limit is the same as with a 1 µF BP/M pin capacitor (reduced current limit value).

G. This parameter is derived from characterization.

H. This parameter is derived from the change in current limit measured at 1X and 4X of the di/dt shown in the I_{LIMIT} specification.

I. I_{DSS1} is the worst case OFF state leakage specification at 80% of BV_{DSS} and maximum operating junction temperature. I_{DSS2} is a typical specification under worst case application conditions (rectified 265 VAC) for no-load consumption calculations.

J. Breakdown voltage may be checked against minimum BV_{DSS} specification by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

K. Auto-restart on time has the same temperature characteristics as the oscillator (inversely proportional to frequency).

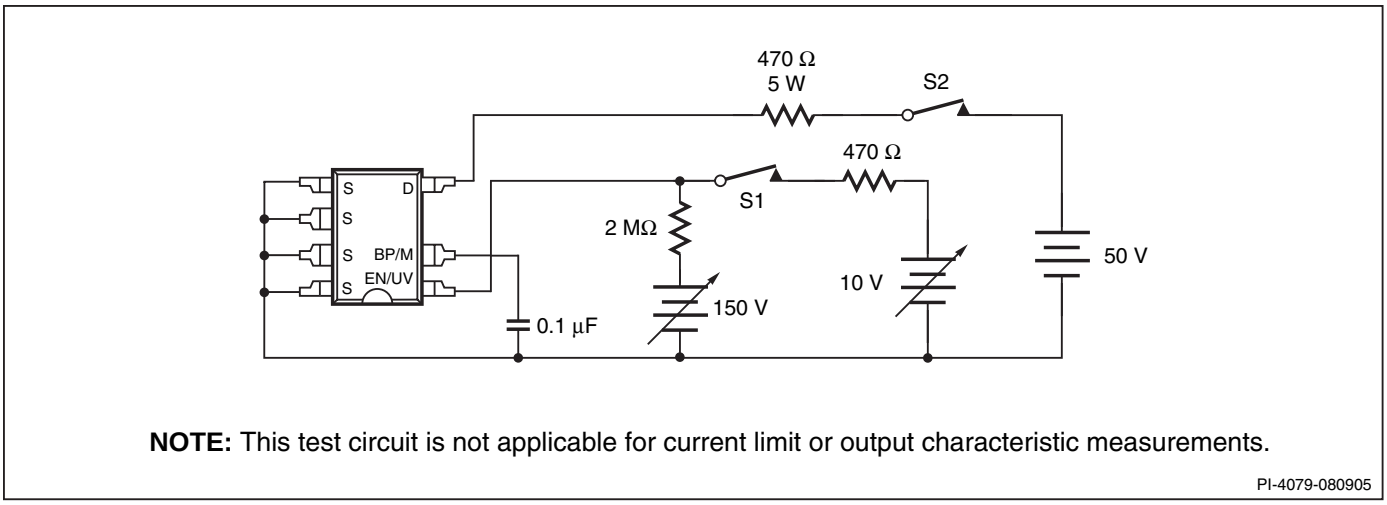


Figure 16. General Test Circuit.

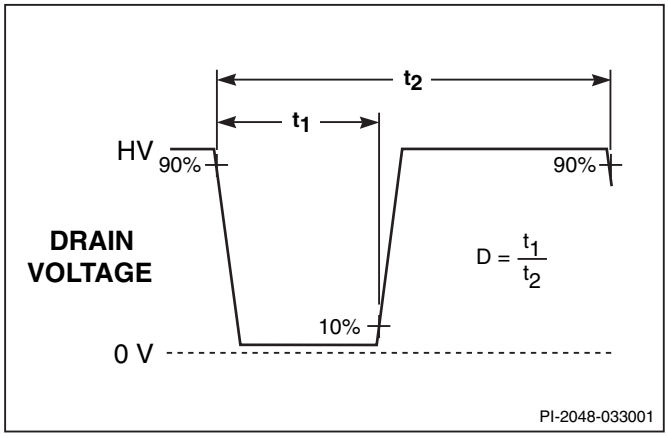


Figure 17. Duty Cycle Measurement.

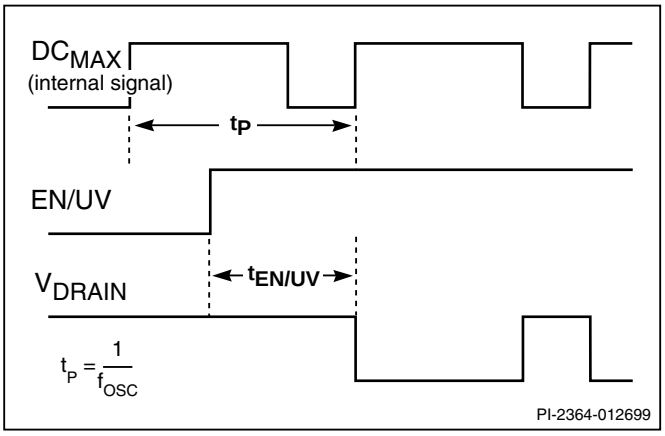


Figure 18. Output Enable Timing.

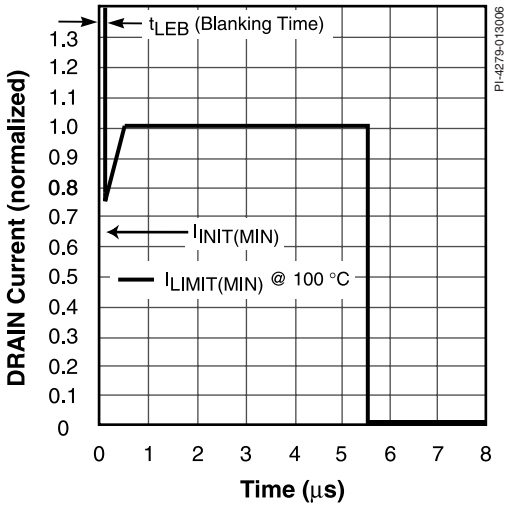


Figure 19. Current Limit Envelope.

Typical Performance Characteristics

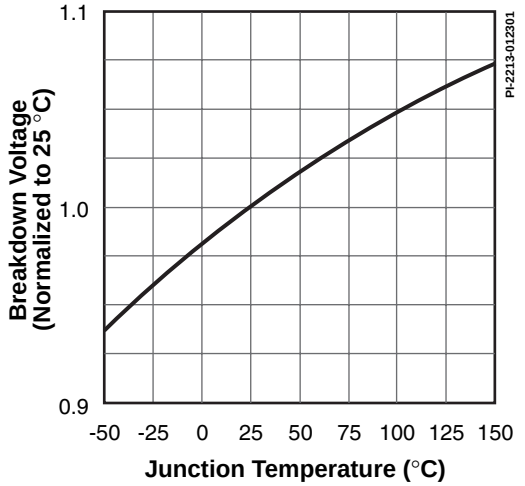


Figure 20. Breakdown vs. Temperature.

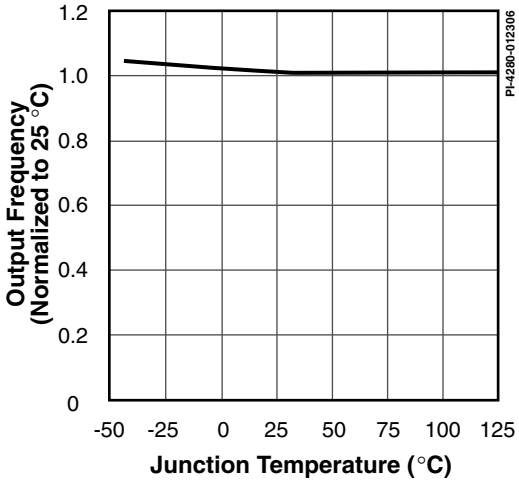


Figure 21. Frequency vs. Temperature.

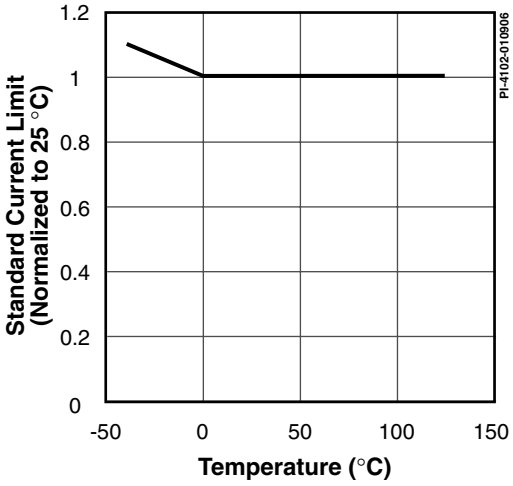


Figure 22. Standard Current Limit vs. Temperature.

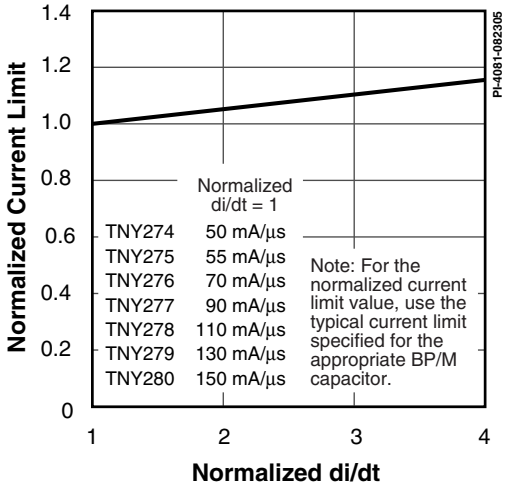


Figure 23. Current Limit vs. di/dt.

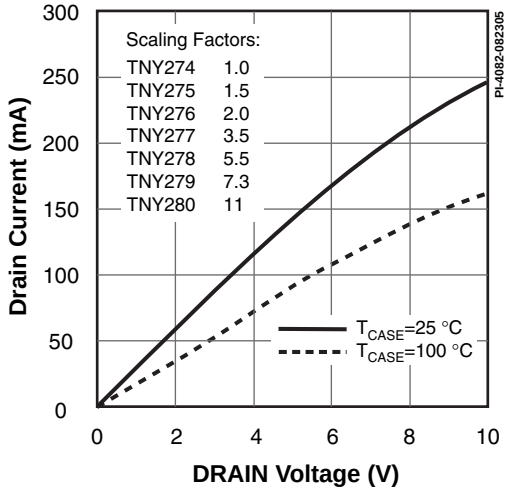


Figure 24. Output Characteristic.

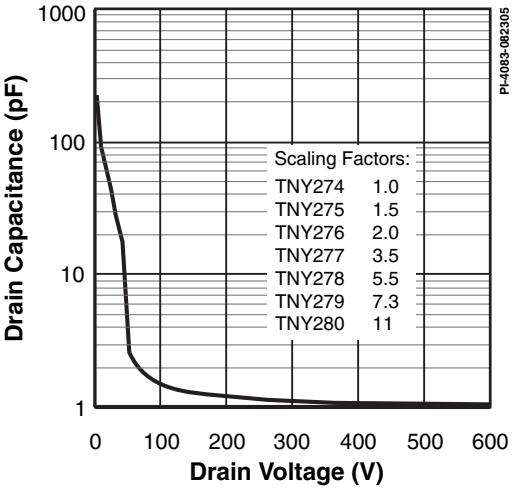


Figure 25. C_{OSS} vs. Drain Voltage.

Typical Performance Characteristics (cont.)

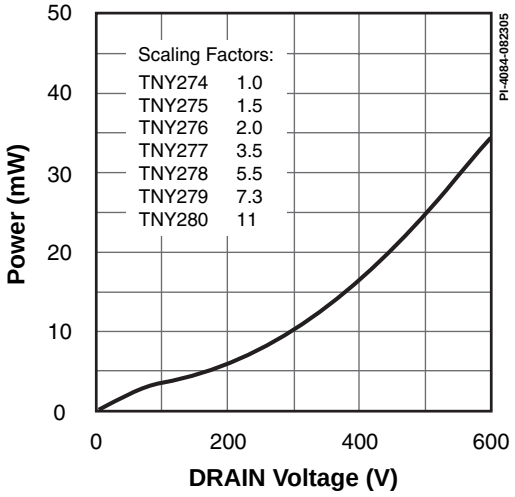


Figure 26. Drain Capacitance Power.

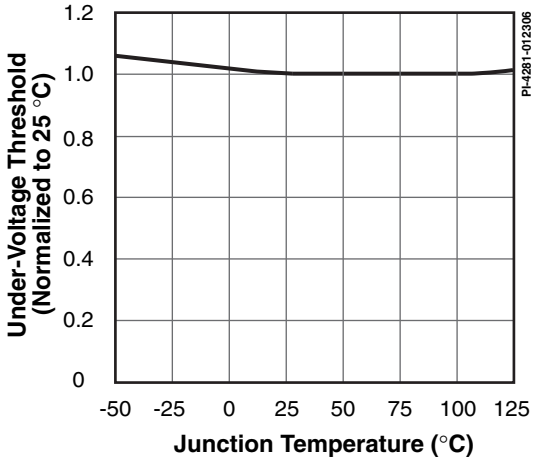
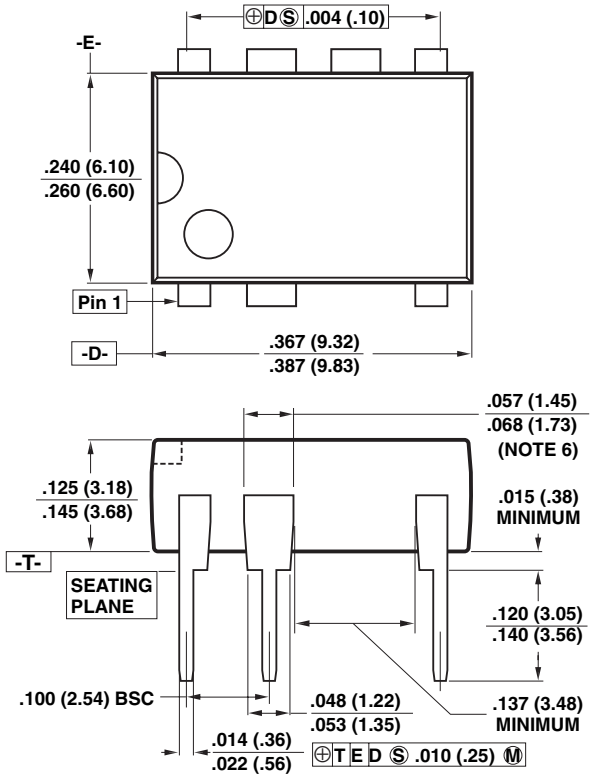


Figure 27. Undervoltage Threshold vs. Temperature.

PART ORDERING INFORMATION

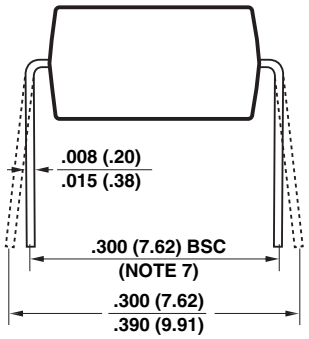
TNY 278 G N - TL	***TinySwitch* Product Family**	
	Series Number	
	Package Identifier	
	G	Plastic Surface Mount SMD-8C
	P	Plastic DIP-8C
	Lead Finish	
	N	Pure Matte Tin (Pb-Free)
	Tape & Reel and Other Options	
	Blank	Standard Configurations
	TL	Tape & Reel, 1000 pcs min./mult., G Package only

DIP-8C



Notes:

1. **Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.**
2. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 3 is omitted.**
5. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
6. **Lead width measured at package body.**
7. **Lead spacing measured with the leads constrained to be perpendicular to plane T.**



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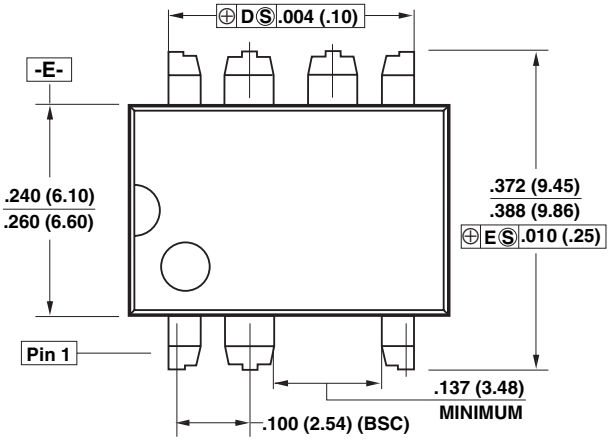
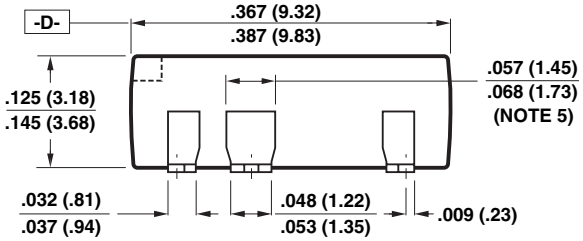
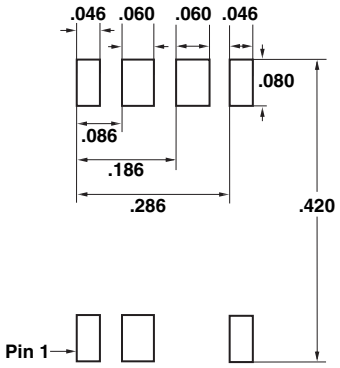
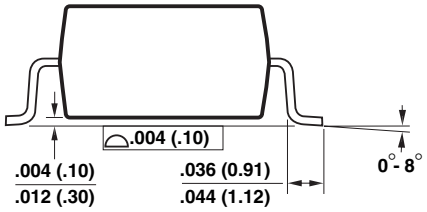






Solder Pad Dimensions



Notes:

1. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
2. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
3. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 3 is omitted.**
4. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
5. **Lead width measured at package body.**
6. **D and E are referenced datums on the package body.**

G08C

PI-4015-013106

Revision	Notes	Date
D	Release final data sheet.	1/06
E	Corrected figure numbers and references.	2/06
F	Seperated current limit and power coefficient values for G package and updated Figure 15. Added EN/UV and PC board leakage currents in Key Applications Considerations section.	4/06
G	Updated line undervoltage current threshold to 2 µA.	6/06

www.powerint.com

Power Integrations Worldwide Sales Support Locations

5245 Hellyer Avenue
San Jose, CA 95138, USA.
Main: +1-408-414-9200
Customer Service:
Phone: +1-408-414-9665
Fax: +1-408-414-9765
e-mail: usasales@powerint.com

Rueckertstrasse 3
D-80336, Munich
Germany
Phone: +49-89-5527-3910
Fax: +49-89-5527-3920
e-mail: eurosales@powerint.com

1st Bldg Shin-Yokohama
2-12-20 Kohoku-ku,
Yokohama-shi, Kanagawa
ken, Japan 222-0033
Phone: +81-45-471-1021
Fax: +81-45-471-3717
e-mail: japansales@powerint.com

5F, No. 318, Nei Hu Rd., Sec. 1
Nei Hu Dist.
Taipei, Taiwan 114, R.O.C.
Phone: +886-2-2659-4570
Fax: +886-2-2659-4550
e-mail: taiwansales@powerint.com

Rm 807-808A
Pacheer Commercial Centre,
555 Nanjing Rd. West
Shanghai, P.R.C. 200041
Phone: +86-21-6215-5548
Fax: +86-21-6215-2468
e-mail: chinasales@powerint.com

#1, 14th Main Road
Vasanthanagar
Bangalore-560052 India
Phone: +91-80-41138020
Fax: +91-80-41138023
e-mail: indiasales@powerint.com

RM 602, 6FL
Korea City Air Terminal B/D, 159-6
Samsung-Dong, Kangnam-Gu,
Seoul, 135-728, Korea
Phone: +82-2-2016-6610
Fax: +82-2-2016-6630
e-mail: koreasales@powerint.com

1st Floor, St. James's House
East Street, Farnham
Surrey GU9 7TJ
United Kingdom
Phone: +44 (0) 1252-730-140
Fax: +44 (0) 1252-727-689
e-mail: eurosales@powerint.com

Rm 2206-2207, Block A,
Electronics Science & Technology Bldg.
2070 Shennan Zhong Rd.
Shenzhen, Guangdong,
China, 518031
Phone: +86-755-8379-3243
Fax: +86-755-8379-5828
e-mail: chinasales@powerint.com

Via De Amicis 2
20091 Bresso MI – Italy
Phone: +39-028-928-6000
Fax: +39-028-928-6009
e-mail: eurosales@powerint.com

51 Newton Road
#15-08/10 Goldhill Plaza
Singapore, 308900
Phone: +65-6358-2160
Fax: +65-6358-2015
e-mail: singaporesales@powerint.com

World Wide +1-408-414-9660

World Wide +1-408-414-9760